CERTIFICATE OF PARTICIPATION

iversity hereby certifies that **Ajinkya Mahajan** has participated in the following course from July 2023 to August 2023:

RTL Design using Verilog

Taught by Prof Vaibhav Taraate.

The participant has successfully completed the course on "RTL Design Using Verilog" with practical assignments, exercises and quizzes. The course covered basics as well as complex RTL Design techniques using Verilog with video sessions on practical design concepts, performance improvement, Finite State Machines and complex design techniques. Following are the details of the broad course contents:

1. Introduction to Design Flow and HDL
2. Concurrency and continuous Assignments
3. Procedural always block and Combinational Design
4. RTL Design for Combinational Logic and Guidelines
5. Verification and Testbenches
6. Sequential Design using Verilog Constructs
7. Other important constructs useful during design and verification
8. RTL design Guidelines
9. Finite State Machines
10. Performance Improvement at RTL Level
11. Complex designs and Strategies while coding the RTL

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